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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,671	08/07/2001	Shigeki Furuya	60188-084	1398

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/922,671	Applicant(s) FURUYA ET AL.	
	Examiner Matthew E. Warren	Art Unit 2815	MW

-- The MAILING DATE of this communication app ars on the cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-51* is/are pending in the application.

4a) Of the above claim(s) *47-51* is/are withdrawn from consideration.

5)☒ Claim(s) *34-40* is/are allowed.

6)☒ Claim(s) *22-33 and 42-46* is/are rejected.

7)☒ Claim(s) *41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Amendment filed on August 1, 2003.

Election/Restrictions

Newly submitted claims 47-51 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the newly submitted claims 47-51 pertain to a method of making semiconductor while the original claims pertain to a semiconductor device.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 47-51 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

Claim 41 is objected to because of the following informalities: lines 14 and 18 of the claim contain the limitation of "the first bent portion and second bent portion..." The is a lack of antecedent basis for the term "portion." Previous recitations of the limitations include a "first bent part." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 42-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "interconnect pattern which is capable of being electrically isolated" is rendered indefinite because of the term "capable." The term "capable" does not specifically recite how the interconnect pattern is connected and denotes that the interconnect pattern might be or might not be electrically isolated from the N or P channel transistor and does not clearly define how the interconnect pattern is connected within the device. The novelty of the invention as understood by the examiner is that the interconnect pattern is electrically isolated from the transistor. The term "capable" leaves the possibility that the interconnect is not isolated from the transistor, in which case the limitation is not supported by the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Manabe (US 6,326,651 B1).

In re claim 22, Manabe shows (fig. 4) a CMOS basic cell comprising an N-channel transistor region (112B) and a P-channel transistor region (112A) isolated from each other by an insulating film (103) on a substrate (1). An interconnect (124 or 123) is connected to one of the N-channel or P-channel transistors through a contact hole. An interconnect pattern (136) exists between the two transistors and is formed in an uppermost interconnect layer (on top of layer 132).

In re claim 23, the interconnect also extends along a direction horizontal to a boundary between the N-channel transistor region and the P-channel transistor region.

Claims 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Amishiro et al. (US 6,288,477 B1).

In re claim 22, Amishiro et al. shows (fig. 5) a CMOS basic cell comprising an N-channel transistor region and a P-channel transistor region (5a and 5b) isolated from each other by an insulating film (2) on a substrate (1). An interconnect (9b or 9c) is connected to one of the N-channel or P-channel transistors through a contact hole. An interconnect pattern (19c) exists between the two transistors and is formed in an uppermost interconnect layer (18).

In re claim 23, Amishiro et al. shows (fig. 5) that the interconnect also extends along a direction horizontal to a boundary between the N-channel transistor region and the P-channel transistor region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manabe (US 6,326,651 B1) in view of the Applicant's Prior Art Figure 31 (APAF).

In re claims 24-27, Manabe does not specifically disclose the power supply and master patterns of the device but is such items are necessary for the function of the semiconductor and well known in the art. However, the APAF 31 also shows a power supply (7), a master pattern , and another interconnect pattern different from the interconnect pattern. The another interconnect patter exists between the N-channel transistor and the master pattern and extends along a perpendicular direction relative to a boundary between two transistors. The another interconnect pattern is disconnected from the transistors and formed in an uppermost interconnect layer. The interconnect is also mutually connected with an interconnect pattern of another CMOS cell, the CMOS cell adjacent to the another CMOS cell. Two or more interconnect patterns are electrically connected by a higher interconnect pattern located in a layer higher than the

interconnect pattern. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the interconnect pattern of Nagai by using power supply and alternate interconnect patterns as shown by the APAF to form connections to the various basic cells in the semiconductor device.

In re claims 28-33, Manabe discloses (col. 6, line 55 – col. 8, line 11) a method of arranging the plurality of CMOS basic cells. However Manabe and the APAF does not show the other methods of realizing the logic circuit. The limitations of claims 28-33 are considered product by process limitations. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Allowable Subject Matter

Claims 34-40 are allowed.

The following is an examiner's statement of reasons for allowance: in re claim 34, the prior art references, alone or in combination, do not show a CMOS basic cell comprising a gate of one of N and P channel transistors having a hooked shape including a first bent part at one upper end portion and second bent part in an opposite side direction at a lower end and a diffusion region having a hooked shape having a first bent part at an upper portion and a second bent part in an opposite side direction at a lower portion wherein the upper portion of the gate is bent oppositely to the upper portion of the diffusion region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim 41 contains allowable subject matter. The prior art references, alone or in combination, do not show a semiconductor integrated circuit including a plurality of CMOS basic cells, each cell composed of first and second N-channel transistors and first and second P-channel transistors, wherein the gates of transistors are disposed such that a first bent part of one gate overlaps a second bent part of another gate when viewed along an axis orthogonal to the axis extending parallel to the sideward directions in which the first bent part and the second bent part extend.

Claim 42 contains allowable subject matter. The prior art references, alone or in combination, do not show a semiconductor integrated circuit comprising CMOS basic cells, an interconnect layer formed in an uppermost layer of each of said plurality of cells, said interconnect layer comprising at least one interconnect operative for connecting signals to and from the corresponding CMOS basic cells, an interconnect pattern electrically isolated from N and P channel transistors and disposed between them, wherein said interconnect pattern is formed in the uppermost layer of said CMOS basic cell.

Response to Arguments

Applicant's arguments with respect to claims 22-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew E. Warren
December 1, 2003